Eight Channel ±60V, ±1.0A, Ultrasound Pulser Demoboard

General Description

The HV7350 is a monolithic eight channel, high-speed, high voltage, ultrasound transmitter RTZ pulser. This integrated, high performance circuit is in a single, 8x8x0.9 mm, 56-lead QFN package.

The HV7350 can deliver a guaranteed ±1.0A source and sink current to a capacitive transducer with +/-60V peak to peak voltage. It is designed for portable medical ultrasound imaging and ultrasound NDT applications. It can also be used as a high voltage driver for other piezoelectric or capacitive MEMS transducers, or for test systems as a signal source or pulse signal generators.

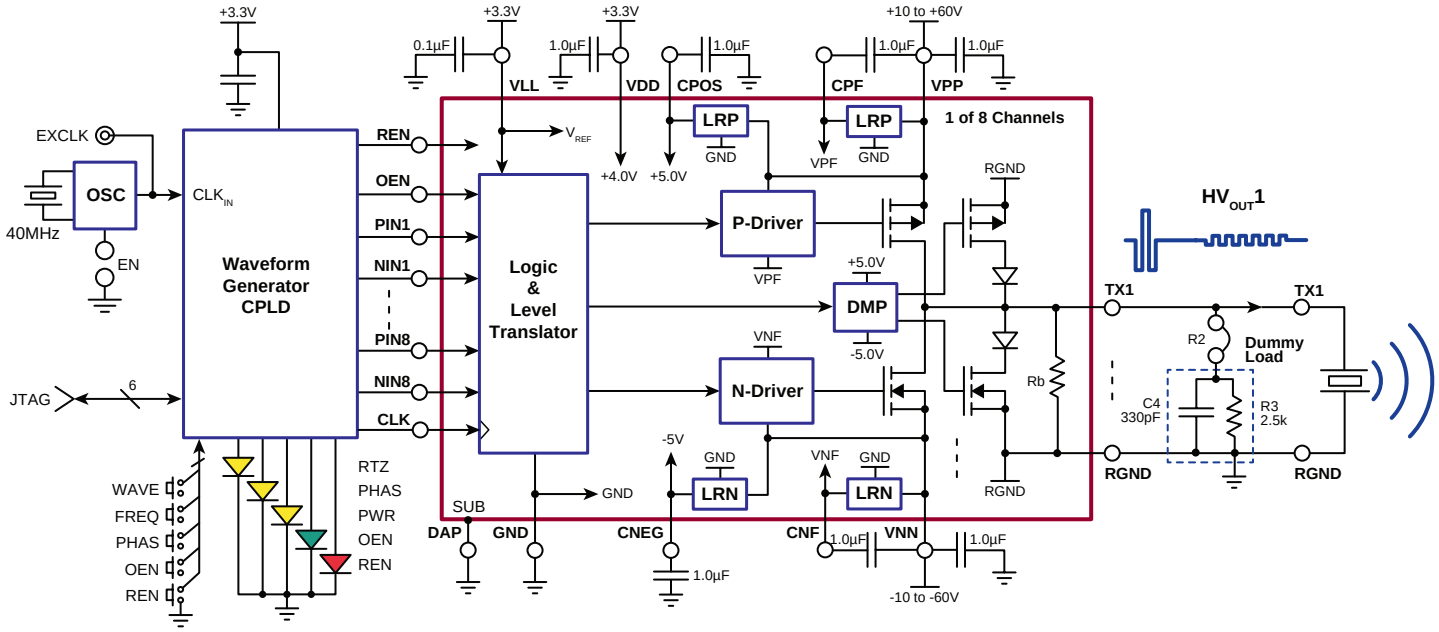
The HV7350's circuitry consists of controller logic circuits, level translators, gate driving buffers and a high current and high voltage MOSFET output stage. The output stages of each channel are designed to provide peak output currents typically over ±1.0A for pulsing, with up to ±60V swings in RTZ mode. The upper limit frequency of the pulser waveform is depending on the load capacitance.

This demoboard datasheet describes how to use the HV7350DB1 to generate the basic high voltage pulse waveform as an ultrasound transmitting pulser.

The HV7350 circuit uses DC coupling from a 3.3V logic input to output Tx1~8 internally, therefore the chip needs three sets of voltage supply rails: V_{LL} +3.3V, V_{DD} +5.0V and V_{PP}/V_{NN} ±10 to ±60V. The V_{PP} and V_{NN} rail voltages can be changed rather quickly, compared to the capacitor gate-coupled driving pulsers. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

The HV7350DB1 output waveforms can be displayed using an oscilloscope by connecting the scope probe directly to the test points TX1~8 and GND. The soldering jumper can select whether or not to connect the on-board dummy-load, a 330pF capacitor paralleling with a 2.5kΩ resistor. The test points can be used to connect the user's transducer to easily evaluate the pulser.

Block Diagram



The PCB Layout Techniques

The large thermal pad at the bottom of the HV7350 package is internally connected to the IC's substrate (VSUB). This thermal pad should be connected to 0V or GND externally on the PCB. Designers need to pay attention to the connecting traces on the outputs TX1~8, specifically the high voltage and high speed traces. In particular, controlled impedance to the ground plane and more trace spacing needs to be applied in this situation.

High speed PCB trace design practices that are compatible with about 50 to 100MHz operating speeds are used for the demoboard PCB layout. The internal circuitry of the HV7350 can operate at quite a high frequency, with the primary speed limitation being load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors and the driver to the FET's gate-coupling capacitors should be as close to the pins as possible. The GND pin should have low inductance feed-through via connections that are connected directly to a solid ground plane. The VDD, VPP, VNN, CPF, CNF, CNEG and CPOS voltage supply and/or bypass capacitor pins can draw fast transient currents of up to ±2.0A, so they should be provided with a low impedance bypass capacitor at the chip's pins. A ceramic capacitor of 1.0 to 2.0µF may be used. Only the VPP and VNN pins to GND capacitors need to be the high-voltage type. The CPF to VPP and CNF to VNN capacitors maybe low voltage. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. For applications that are sensitive to jitter and noise and using multiple HV7350 ICs, insert another ferrite bead between each chip's supply lines.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of the HV7350's high voltage power stages is very low, in some cases it may be desirable to add a small value resistor in series with the output TX1~8 to obtain better waveform integrity at the load terminals after long cables. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Be aware of the parasitic coupling from the outputs to the input signal terminals of the HV7350. This feedback may cause oscillations or spurious waveform shapes on the edges of the signal transitions. Since the input operates with signals down to 3.3V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

Testing the Integrated Pulser

The HV7350 pulser demoboard should be powered up with multiple lab DC power supplies with current limiting functions.

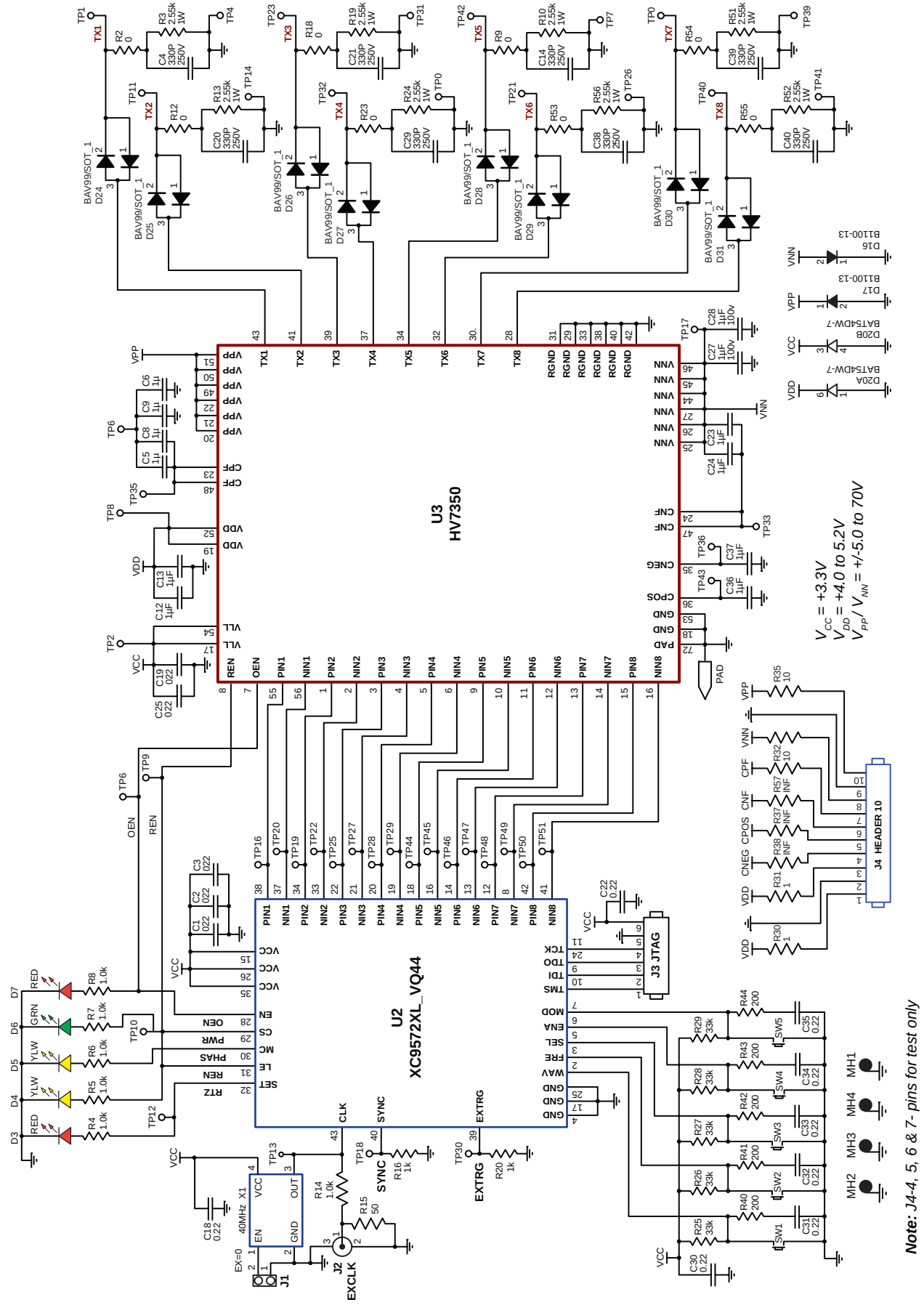
The on-board dummy load 330pF//2.5kΩ should be connected to the high voltage pulser output through the solder jumper when using an oscilloscope's high impedance probe to meet the typical loading condition. To evaluate different loading conditions, one may change the values of RC within the current and power limit of the device.

In order to drive the user's piezo transducers with a cable, one should match the output load impendence properly to avoid cable and transducer reflections. A 70 to 75Ω coaxial cable is recommended. The coaxial cable end should be soldered to the TX1~8 and GND directly with very short leads. If a user's load is being used, the on-board dummy load should be disconnected by cutting the small shorting copper trace in between the 0Ω resistors R2, R9, R12, R18, R23, R53, R54 or R55 pads. They are shorted by factory default.

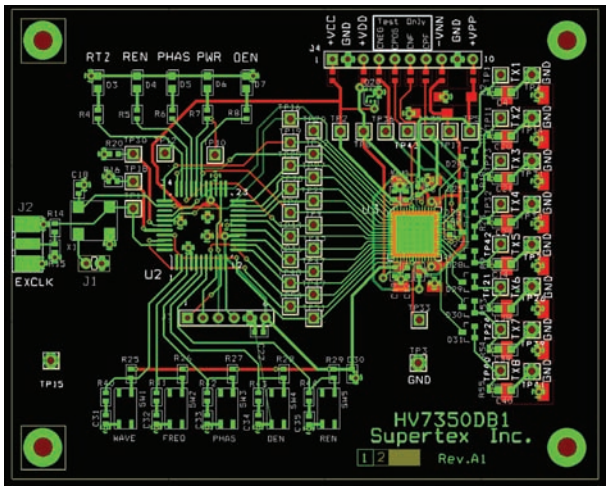
All the on-board test points are designed to work with the high impedance probe of the oscilloscope. Some probes may have limited input voltage. When using the probe on these high voltage test-points, make sure that V_{PP}/V_{NN} voltages do not exceed the probe limit. Using the high impendence oscilloscope probe for the on-board test points, it is important to have short ground leads to the circuit board ground plane.

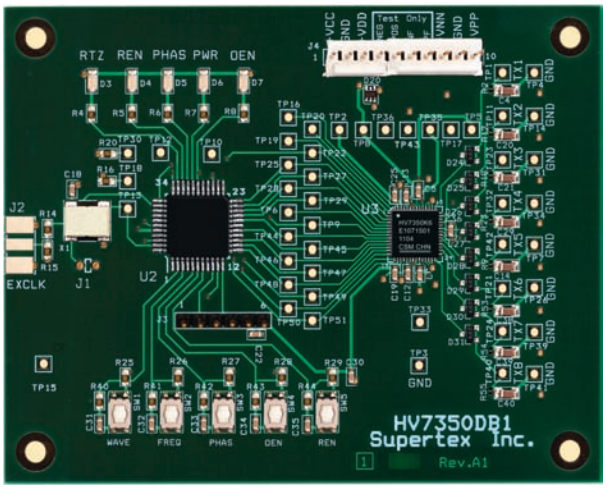
If both of the inputs PIN and NIN are high, then the channel out TX will be in Hi-Z.

HV7350DB1 Schematic



HV7350DB1 PCB and Board Layout





Actual Board Size: 72.4mm x 68.4mm

Power Connector Description

1	$+V_{CC}$	+3.3V Logic voltage input for V_{LL} and CPLD. (100mA)
2	GND	0V, Ground
3	$+V_{DD}$	+5.0V HV7350 positive V_{DD} supply. (25mA)
4	CNEG	-5.0V HV7350 negative V_{NEG} supply, only when REN=0
5	CPOS	+5.0V HV7350 Positive V_{POS} supply, only when REN=0
6	CNF	HV7350 V_{NF} supply reference to V_{NN}, (V_{NF} - V_{NN}) = +5.0V, only when REN=0
7	CPF	HV7350 V_{PF} supply reference to VPP, (V_{PP} - V_{PF}) = +5.0V, only when REN=0
8	$-V_{NN}$	-10 to -60V negative high voltage supply. (-5.0mA)
9	GND	0V, Ground
10	$+V_{PP}$	+10 to +60V positive high voltage supply. (+5.0mA)

Note: *J4-4 to 7 are for external power connection of V_{NEG}, V_{POS}, V_{NF}, V_{PF} when REN = 0. Note, as default the resistors R34, R37, R38 and R57 is not installed. Do not need to connect these four pins to any power supply when internal regulators are be used when REN=1.*

Voltage Supply Power-Up and Operation Sequence

1	$+V_{CC}$	Power on +3.3V positive logic supply voltage for HV7350's V_{LL} and CPLD V_{CC}
2	$+V_{DD}$	Power on +5.0V V_{DD} positive supply
3	OEN & REN	Turn both OEN & REN LED off
4	$+V_{PP}$ / $-V_{NN}$	Power on V_{PP}/V_{NN} = ±10 to 60V positive and negative high voltage supply
5	OEN & REN	Turn on OEN & REN LED on
6	WAVE Button	Push WAVE button to select waveforms

Note: *Power-down in the 6,5… to 1 reversing order.*

Push Button Operations

WAV	Toggle select pulse B-mode waveforms: None, 1-cycle, 1-cycle inverting, 3-cycle & 3-cycle inverting
FREQ	Toggle select B-mode demo frequency of 10, 5, 2.5, 1.25 & 0.625MHz when X1 oscillator is 40MHz
PHAS	Toggle select B-mode waveform phase polarity
OEN	Toggle on or off HV7350 chip output signal OEN
REN	Toggle select on or off HV7350 internal voltage-regulators signal REN

LED Indicator

RTZ	RTZ indication, default is on
PHAS	Phase polarity indication
PWR	HV7350DB1 V_{LL} 3.3V and CPLD chip V_{CC} power supply indication
OEN	HV7350 chip enable EN signal indication, power on default is off until OEN button is pushed
REN	HV7350 built-in regulators enable indication, power on default is off until REN button is pushed

Typical Waveforms

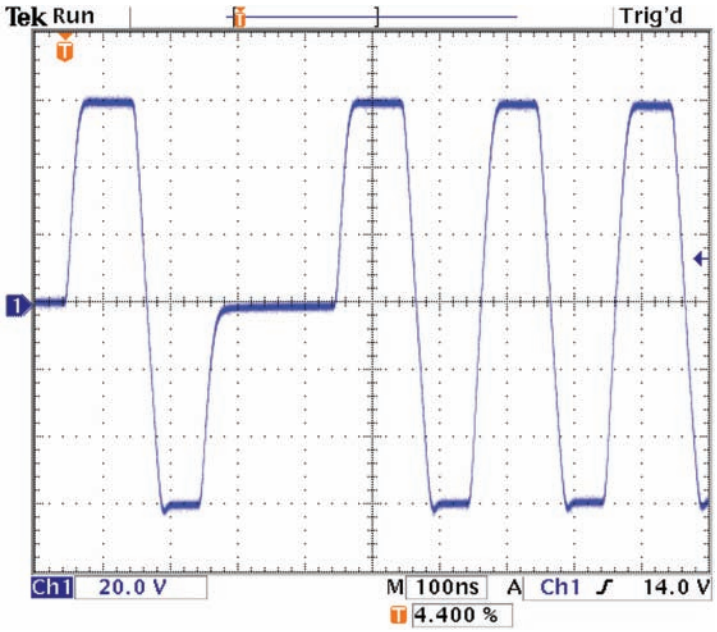


Figure 1. V_{PP}/V_{NN} = +/-60V 5MHz with 330pF//2.5kΩ load and 8-Channel pulsing

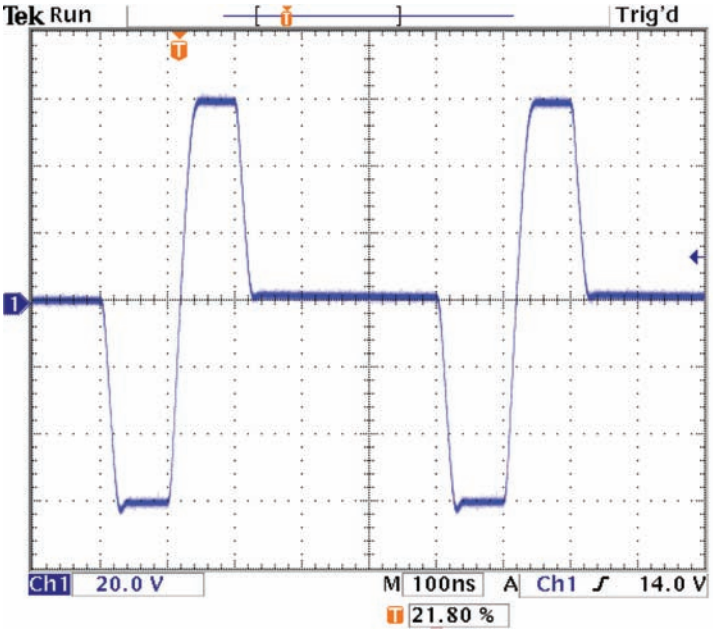


Figure 2. V_{PP}/V_{NN} = +/-60V 5MHz with 330pF//2.5kΩ load and 8-Channel pulsing

Typical Waveforms *(cont.)*

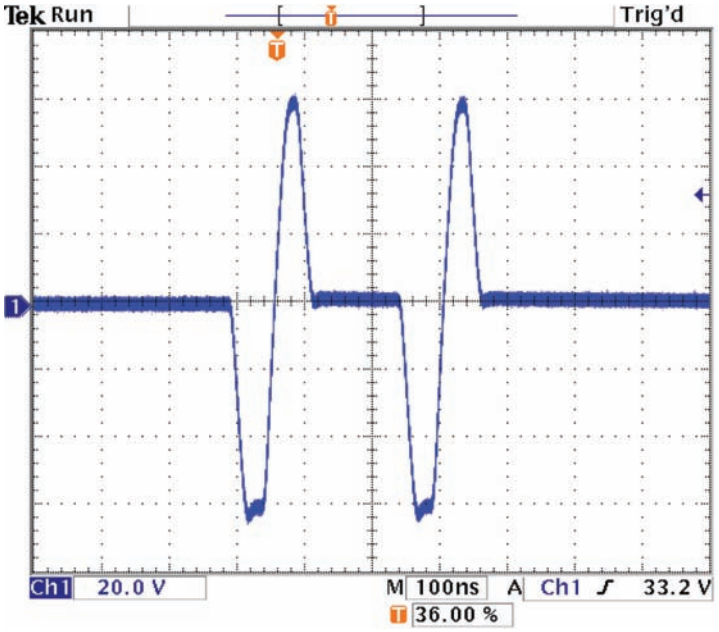


Figure 3. V_{PP}/V_{NN} = +/-60V 10MHz with 330pF//2.5kΩ load and 8-Channel pulsing

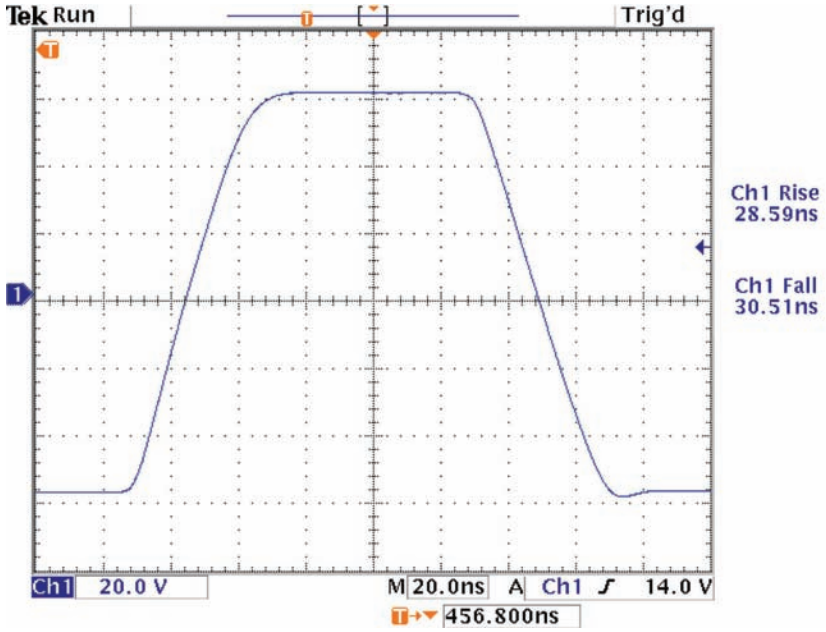


Figure. 4. Rise and Fall time at V_{PP}/V_{NN} = +/-60V with 330pF//2.5kΩ load

Typical Waveforms *(cont.)*

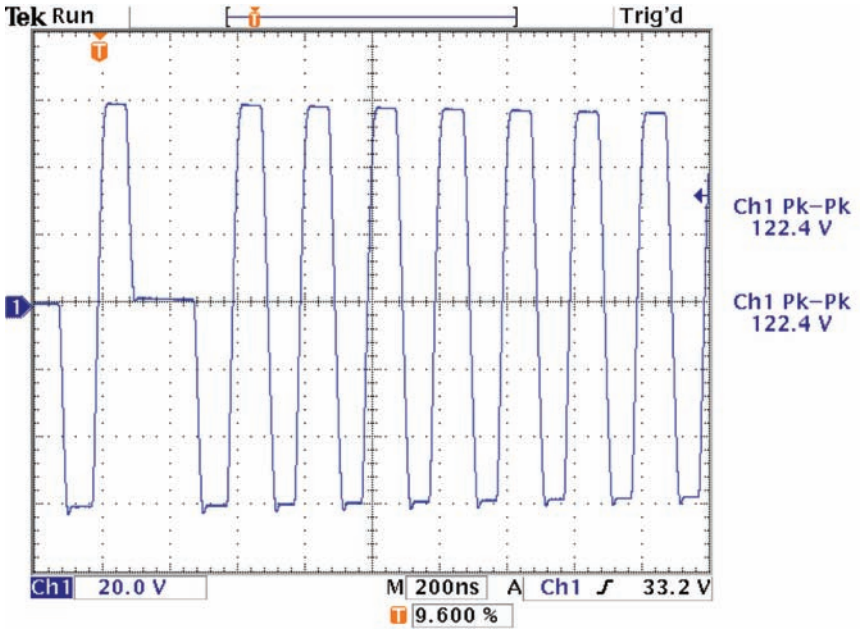


Figure 5. V_{PP}/V_{NN} = +/-60V 5MHz with 330pF//2.5kΩ load and 8-Channel pulsing

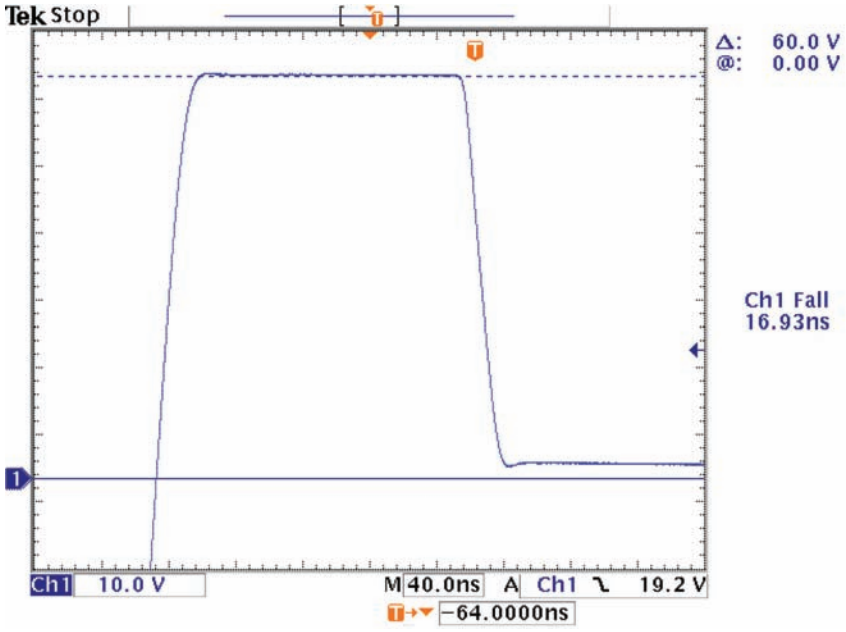


Figure 6. Damping fall time at V_{PP}/V_{NN} = +/-60V with 330pF//2.5kΩ load

Typical Waveforms *(cont.)*

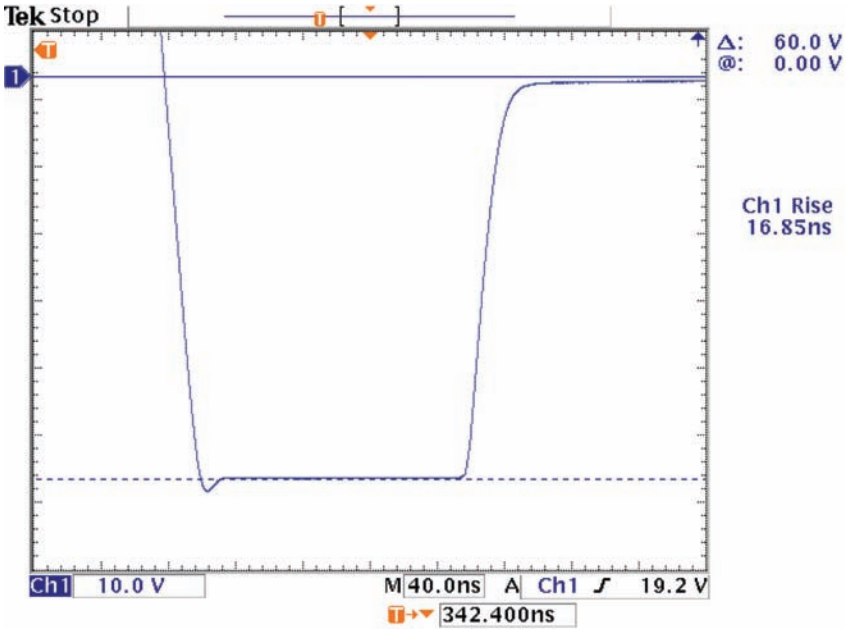


Figure 7. Damping rise time at V_{PP}/V_{NN} = +/-60V with 330pF//2.5kΩ load

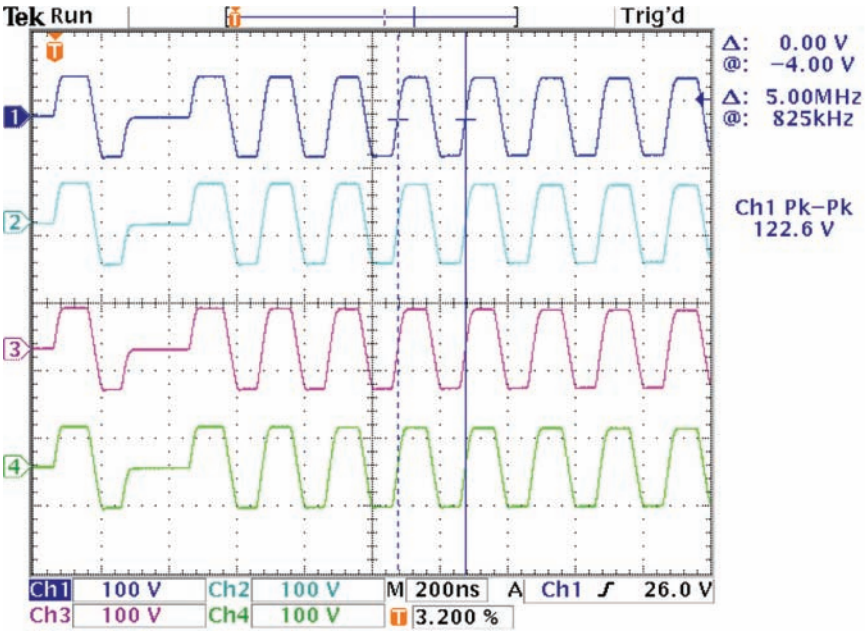


Figure 8. V_{PP}/V_{NN} = +/-60V 5MHz with 330pF//2.5kΩ load 4 of the 8-Channel waveforms shown

Typical Waveforms *(cont.)*

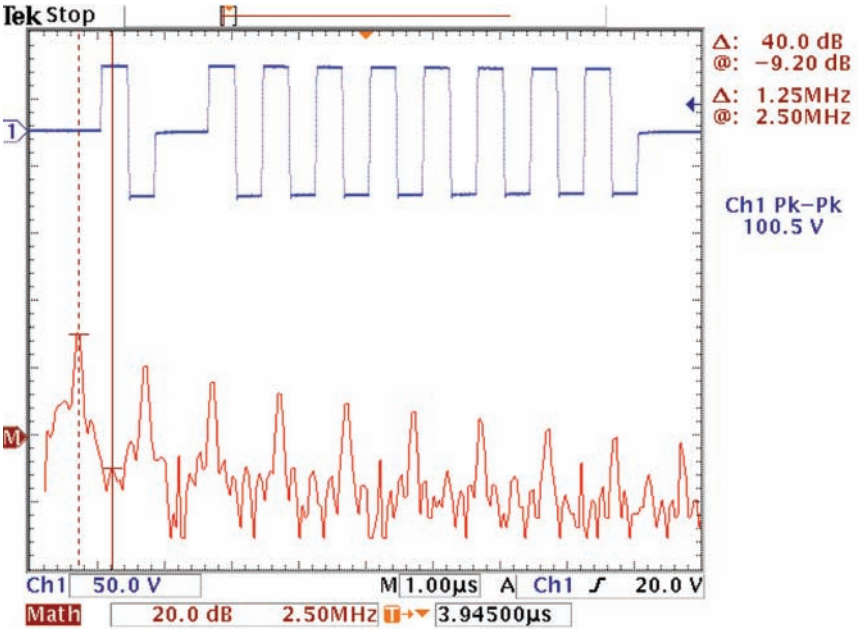


Figure 9. HD2 at V_{PP}/V_{NN} = +/-50V 2.5MHz with 330pF//2.5kΩ load

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